Abstract of the Disclosure:

An integrated memory circuit has a memory cell array and a test circuit. The test circuit generates an assessment datum, the assessment datum is dependent on a result of a comparison between a datum read from the memory cell array and a datum previously written to the memory cell array. A coding unit is coupled to the test circuit in order to code a plurality of assessment signals to form a coded test signal, a voltage signal is assigned to the plurality of test data as coded test datum.

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